AMENDMENTS TO THE CLAIMS

1. (currently amended) An NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;

a nanolaminate gate dielectric formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric comprising a composition of one of atomic layer deposition (ALD) Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD ZrO_2 – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD HfO_2 – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated HfO_2 – ALD Lanthanide Oxide; and

a control gate formed on top of the gate dielectric.

2 – 3 (canceled)

4. (original) The transistor of claim 2 wherein the gate dielectric has a larger energy barrier between the high-k dielectric and the oxide insulator than silicon dioxide.

5. (canceled)

6. (original) An NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises one of atomic layer deposition (ALD) Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD ZrO_2 – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD HfO_2 – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated HfO_2 – ALD Lanthanide Oxide; and

a control gate formed on top of the gate insulator layer.

7. (canceled)

8. (original) The transistor of claim 6 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.

9. (original) The transistor of claim 6 wherein the control gate is a polysilicon material.

10. (original) The transistor of claim 6 wherein the substrate is comprised of a p+ type silicon material.

11 – 14 (canceled)

15. (currently amended) An electronic system comprising:

a processor that generates control signals; and

a memory array coupled to the processor, the array comprising a plurality of NROM memory cells, each NROM memory cell comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a nanolaminate gate dielectric formed on top of the substrate substantially between each pair of the plurality of source/drain regions, the gate dielectric comprises one of atomic layer deposition (ALD) Lanthanide (Pr, Ne, Sm, Gd, and Dy) Oxide – ALD ZrO_2 – ALD Lanthanide Oxide, ALD Lanthanide Oxide – ALD HfO_2 – ALD Lanthanide Oxide, or ALD Lanthanide Oxide – evaporated HfO_2 – ALD Lanthanide Oxide; and

a control gate formed on top of the oxide insulator.

16-34 (canceled)